ABSTRACT

A decoder structure is described that can be implemented on an integrated circuit and used to decode turbo codes. A soft input soft output decoder includes a metric aggregator, and a codeword resolver, each of these elements co-operating to resolve manipulated branch and state metric pairs to a codeword in a known set of codewords in accordance with an un-normalized likelihood relationship between the received branch and state metric data pairs and the known set of codewords. The present invention is believed to operate at a relatively lower clock speed and occupy a relatively smaller area than previous structures, thereby consuming less power and incurring lower cost to produce, yet still achieve a substantially similar BER performance. The present invention is suitable for extremely high data rate communications; for example, rates in excess of 100 Mbit/s, such as at 200 MHz and 220 MHz, can be achieved.